

**freescale**
semiconductor**FACSIMILE****LAW DEPARTMENT
FREESCALE SEMICONDUCTOR, INC.****DATE:** January 29, 2007**TO:** MS: ISSUE FEE (571) 272-2885
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(LOCATION) (FAX NUMBER)**FROM:** Stacie Herrera for James L. Clingan, Jr. (512) 996-6848
(SENDER) (EXTENSION)**TOTAL NUMBER OF PAGES** 5 (including this page)IF YOU HAVE ANY TROUBLE OR QUESTIONS WITH TRANSMISSION, OR HAVE RECEIVED IT IN
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Docket No.: SC13265TP

Applicant: Alexander L. Barr

Serial No.: 10/780,143

Art Unit: 2823

Filed: February 17, 2004

ALL ITEMS MARKED WITH AN "X" ARE INCLUDED:

1.	<input checked="" type="checkbox"/>	1 page Facsimile Cover Sheet
2.	<input checked="" type="checkbox"/>	1 page PTOL-85B Issue Fee Transmittal (in duplicate)
3.	<input checked="" type="checkbox"/>	2 page Comments on Statement for Reasons of Allowance

Paid by Deposit Account 503079, Freescale Semiconductor, Inc: \$1700

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby
authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.**I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS
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UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S) Alexander L. Barr et al GROUP ART UNIT: 2823
APPLN. NO.: 10/780,143 EXAMINER: William D. Coleman
FILED: February 17, 2004
TITLE: SEMICONDUCTOR STRUCTURE HAVING STRAINED
SEMICONDUCTOR AND METHOD THEREFOR

Certificate of Submission

I hereby certify that this correspondence is being submitted to the U.S.P.T.O.,
Alexandria, VA.

- ☐ Addressed per C.F.R. § 1.1(a) and deposited with the United States Postal
Service with sufficient postage as first class mail.
- ☒ Facsimile transmitted in accordance with C.F.R. § 1.6(d).
- ☐ Submitted electronically via EFS in accordance with "Legal Framework
for EFS Web".

1-29-07

Date of Submission

/Stacie Herrera/
Signature

Stacie Herrera

Printed Name of Person Signing Certificate

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is filed contemporaneous with the filing of the issue fee for this application.
Entrance of the comments provided below regarding the statement of reasons for allowance
provided by the Examiner is respectfully requested.

REMARKS

The Examiner's reasons for allowance apply to claim 1 with the "a" between "layer" and "aligning" changed to "and." This comment is generally applicable to claim 14 also but claim 14 identifies the layer being cleaved as SiGe. Applicants, however, cannot agree that the Examiner's characterization applies to claims 7, 9-12, 15, 17, 19-22, and 24. For example, independent claims 7 and 15 do not specify cleaving.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125

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